

# MARK W. WILSON

PARTNER

503.473.0876 | mark.wilson@klarquist.com



## OVERVIEW

Mark focuses on the preparation and prosecution of patent applications in the electrical engineering and computer science fields. His practice also includes prosecuting and defending patent post-grant review proceedings, assisting with domestic and foreign patent litigation (including infringement and invalidity analysis and discovery), and counseling clients regarding patent infringement and validity.

Mark has 11 years of experience developing electronic design automation (EDA) software tools and related methodologies for high performance integrated circuit designs. His technical expertise spans a number of fields in the electrical engineering and computer science disciplines, including VLSI design, analog and digital circuits, semiconductors, signal processing, power and control systems, computer graphics, and software engineering. Mark also has experience preparing and prosecuting patent applications in the mechanical, nanotechnology, and business method arts.

Mark first joined Klarquist as a summer associate in 2007, returned as an associate in 2008, and became partner in 2016.

## PROFESSIONAL EXPERIENCE

► Intel | 1995 – 2007 | Hillsboro, OR

*While at Intel, Mark developed design and verification EDA tools for leading-edge deep submicron designs, including the Intel Pentium® II, Pentium® 4, and Core™ i7 microprocessors. In addition, he managed a team of design automation engineers, and served as an invention disclosure reviewer for the Intel Legal Software IP committee.*

► Carnegie Mellon Research Institute | 1993 – 1994 | Pittsburgh, PA

*Designed, built, and tested wired and wireless industrial control and solid state gas sensor prototypes.*

## EDUCATION

J.D., cum laude, Lewis & Clark Law School, 2008

B.S., Electrical and Computer Engineering, Carnegie Mellon University, 1995

## ADMISSIONS

Oregon, 2009

U.S. Patent and Trademark Office, 2008 (Reg. No. 63,126)

U.S. District Court for the District of Oregon

## PRACTICE AREAS

Patents

Post-Grant USPTO Proceedings

Litigation

Intellectual Property Counseling

## TECHNOLOGY AREAS

Electrical & Semiconductors

Software & Internet Technology

Nanotechnology

Mechanical

**Klarquist**

# MARK W. WILSON

PARTNER

503.473.0876 | mark.wilson@klarquist.com

---

## HONORS & AWARDS

- ▶ *IAM Patent 1000: The World's Leading Patent Professionals* | 2022
  - ▶ Oregon Super Lawyers® Rising Star | 2017 - 2020
  - ▶ Three Intel Division Awards (outstanding execution in layout verification and tapeout for a 90 nm microprocessor (2003), analysis and implementation of layout fixes for yield increase for a 0.18 μm processor (2001), and development of an incremental parameterized standard cell layout methodology (2007))
- 

## PRESENTATIONS & PUBLICATIONS

- ▶ Patent Eligibility Practice Considerations for Software, CLE Presentation, Battelle Memorial Institute, June 2014.
- ▶ Drafting Invalidity and Non-infringement Opinions, CLE presentation, Klarquist Sparkman, LLP, January 2013.
- ▶ Post-Grant Proceedings after the AIA, CLE presentation, Tonkon Torp, LLP, November 2012.
- ▶ Why Private Remedies for Environmental Torts Under the Alien Tort Statute Should Not Be Constrained by the Judicially Created Doctrines of Jus Cogens and Exhaustion, 39 *Env'tl. L.* 451 (2009).
- ▶ Co-authored three papers for the Intel Design & Test Technology conference, including: Novel Features & Methodology to Increase Physical Design for Debug Coverage by 10X, Rapid Interconnect Design Through the Use of Virtual Repeaters, and Willamette Stretchable Cell Layout Methodology.