MARK W. WILSON

PARTNER
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OVERVIEW

Mark focuses on solving intellectual property problems for clients in the electrical engineering and computer science technical fields. His practice includes patent litigation, client counseling, and patent prosecution. He has significant experience with post grant proceedings and examinations.

Mark has 11 years of experience developing electronic design automation (EDA) software tools and methodologies for high performance integrated circuit designs. His technical expertise spans a number of fields in the electrical engineering and computer science disciplines, including integrated circuit architecture, design, and layout; semiconductor manufacturing and testing, signal processing, power and control systems, computer graphics, and software engineering. Mark also has experience preparing and prosecuting patent applications in the mechanical, nanotechnology, and business method arts.

Mark first joined Klarquist as a summer associate in 2007, returned as an associate in 2008, and became partner in 2016.

PROFESSIONAL EXPERIENCE

- Intel | 1995 – 2007 | Hillsboro, OR

While at Intel, Mark developed design and verification EDA tools for leading-edge deep submicron designs, including the Intel Pentium® II, Pentium® 4, and Core™ i7 microprocessors. In addition, he managed a team of design automation engineers, and served as an invention disclosure reviewer for the Intel Legal Software IP committee.

- Carnegie Mellon Research Institute | 1993 – 1994 | Pittsburgh, PA

Designed, built, and tested wired and wireless industrial control and solid state gas sensor prototypes.

EDUCATION

J.D., *cum laude*, Lewis & Clark Law School, 2008

B.S., Electrical and Computer Engineering, Carnegie Mellon University, 1995

ADMISSIONS

Oregon, 2009

U.S. Patent and Trademark Office, 2008 (Reg. No. 63,126)

U.S. District Court for the District of Oregon

U.S. District Court for the Eastern District of Texas

U.S. Court of Appeals for the Federal Circuit

PRACTICE AREAS

Patents

Post-Grant USPTO Proceedings

Litigation

Intellectual Property Counseling

TECHNOLOGY AREAS

Electrical & Semiconductors

Software & Internet Technology

Klarquist

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HONORS & AWARDS

- *IAM Patent 1000: The World's Leading Patent Professionals* | 2022, 2023
- Oregon Super Lawyers® Rising Star | 2017 - 2020
- Three Intel Division Awards (outstanding execution in layout verification and tapeout for a 90 nm microprocessor (2003), analysis and implementation of layout fixes for yield increase for a 0.18 µm processor (2001), and development of an incremental parameterized standard cell layout methodology (2007))

PROFESSIONAL ACTIVITIES

- Chair, Oregon State Bar IP Section; 2021 Executive Committee 2017-2022
- Member, American Intellectual Property Law Association
- Member, Oregon Patent Law Association
- Member, Association of Computing Machinery

PRESENTATIONS & PUBLICATIONS

- Patent Eligibility Practice Considerations for Software, CLE Presentation, Battelle Memorial Institute, June 2014.
- Drafting Invalidity and Non-infringement Opinions, CLE presentation, Klarquist Sparkman, LLP, January 2013.
- Post-Grant Proceedings after the AIA, CLE presentation, Tonkon Torp, LLP, November 2012.
- Why Private Remedies for Environmental Torts Under the Alien Tort Statute Should Not Be Constrained by the Judicially Created Doctrines of Jus Cogens and Exhaustion, 39 Envtl. L. 451 (2009).
- Co-authored three papers for the Intel Design & Test Technology conference, including: Novel Features & Methodology to Increase Physical Design for Debug Coverage by 10X, Rapid Interconnect Design Through the Use of Virtual Repeaters, and Willamette Stretchable Cell Layout Methodology.