Mark W. Wilson

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PRACTICE AREAS

Intellectual Property Counseling
Patents
Litigation
Outsourced "In-House" IP Counsel
Post-Grant USPTO Proceedings
Startups & Emerging Businesses

TECHNOLOGIES

Electrical & Semiconductors
Mechanical
Nanotechnology
Software & Internet Technology

PRACTICE AREA OVERVIEW

Mr. Wilson focuses on the preparation and prosecution of patent applications in the electrical engineering and computer science fields. His practice also includes prosecuting and defending patent post-grant review proceedings, assisting with domestic and foreign patent litigation (including infringement and invalidity analysis and discovery), and counseling clients regarding patent infringement and validity.

TECHNICAL EXPERTISE

Mr. Wilson has eleven years of experience developing electronic design automation (EDA) software tools and related methodologies for high performance integrated circuit designs. His technical expertise spans a number of fields in the electrical engineering and computer science disciplines, including VLSI design, analog and digital circuits, semiconductors, signal processing, power and control systems, computer graphics, and software engineering. Mr. Wilson also has experience preparing and prosecuting patent applications in the mechanical, nanotechnology, and business method arts.

PRIOR PROFESSIONAL EXPERIENCE

Intel Corporation, Hillsboro, OR | 1995 - 2007
While at Intel, Mr. Wilson developed design and verification EDA tools for leading-edge deep submicron designs, including the Intel Pentium® II, Pentium® 4, and Core™ i7 microprocessors. In addition, Mr. Wilson managed a team of design automation engineers, and served as an invention disclosure reviewer for the Intel Legal Software IP committee.

Carnegie Mellon Research Institute, Pittsburgh, PA | 1993 - 1994
Mr. Wilson designed, built, and tested wired and wireless industrial control and solid state gas sensor prototypes.

HONORS AND AWARDS

Mr. Wilson received three Intel Division Awards for outstanding execution in layout verification and tapeout for a 90 nm microprocessor, analysis and implementation of layout fixes for yield increase for a 0.18 µm processor, and development of an incremental parameterized standard cell layout methodology.

EDUCATION

- J.D., *cum laude*, Lewis & Clark Law School, 2008
- B.S., Electrical and Computer Engineering, Carnegie Mellon University, 1995

BAR ADMISSIONS

- Oregon, 2009
- U.S. Patent and Trademark Office (Reg. No. 63,126)

COURT ADMISSIONS

- U.S. District Court for the District of Oregon

YEAR JOINED FIRM

2008

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PRESENTATIONS AND PUBLICATIONS

- *Patent Eligibility Practice Considerations for Software*, CLE Presentation, Battelle Memorial Institute, June 2014.

- *Portland Business Journal*, Ask the Legal Professional, October 2013

- *Drafting Invalidity and Non-infringement Opinions*, CLE presentation, Klarquist Sparkman, LLP, January 2013.

- *Post-Grant Proceedings after the AIA*, CLE presentation, Tonkon Torp, LLP, November 2012.

- *Why Private Remedies for Environmental Torts Under the Alien Tort Statute Should Not Be Constrained by the Judicially Created Doctrines of Jus Cogens and Exhaustion*, 39 Envtl. L. 451 (2009).

- Mr. Wilson co-authored three papers for the Intel Design & Test Technology conference, including: *Novel Features & Methodology to Increase Physical Design for Debug Coverage by 10X, Rapid Interconnect Design Through the Use of Virtual Repeaters, and Willamette Stretchable Cell Layout Methodology.*